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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,507	03/29/2001	David William Boerstler	AUS920000512US1	5087

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Kelly K. Kordzik
100 Congress Avenue, Suite 800
Austin, TX 78701

EXAMINER	
TSE, YOUNG TOI	
ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,507	BOERSTLER, DAVID WILLIAM	
	Examiner	Art Unit	
	YOUNG T. TSE	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the reference sign "03" shown in Figure 4B should be "Φ3". Further, the block pertaining elements (401A-403E) in Figure 4A and (403A to 403E) in Figure 4B need to have descriptive label, in conformance with 37 CFR 1.84(n) and 1.84(o). For example, a descriptive label of "Flip-Flop" should be inserted into Figure 4A to properly describe element (401A). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the

description: the disclosure of the drawings includes Figure 5A and Figure 5B, however, they are not mentioned in the specification. Further, reference signs "Φ1B", "Φ2B", "Φ3B", "Φ4B" and "Φ5B" shown in Figures 4A and 4B are the complements of "Φ1", "Φ2", "Φ3", "Φ4" and "Φ5" are also not mention in the specification. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: on page 1, lines 5-8, and page 6, line 17, Applicant is requested to update the US serial application numbers and the filing dates; on page 5, line 11, "illustrates" should be "illustrate" and line 13, only Figure 5 is described in the Brief Description of the Drawings, however, Figures 5A and 5B are also shown in the disclosure of the drawings; and on page 11, line 21, "Figure 5" should be "Figure 4A". For the formality of the application under the present office practice, applicant(s) is required to replace "Claims" with "I or We Claim", "The Invention

Claimed Is" (or the equivalent) before the Claims part of the specification of the instant application. See MPEP 608.01(m). Appropriate correction is required.

Claim Objections

3. Claims 1-24 are objected to because of the following informalities: in claim 1, line 4, "said phases of said clock signal, circuitry for receiving serial data, and circuitry" should be "said phases of said clock signal and said serial data, said circuitry" and line 6, "said clock" should be "said clock signal"; in claim 2 (lines 3-4), claim 4 (line 2 and line 3), claim 6 (line 2 and line 3), claim 7 (line 11), claim 8 (line 3), claim 9 (line 2 and line 3), and claim 12 (line 2 and line 3), "said clock" should be "said clock signal"; in claim 2 (line 3) and claim 8 (line 3), "a particular phase" should be "said particular phase" for clarity; in claim 4 (line 4) and claim 10 (line 4), "a value" should be "the value", and in claim 7, lines 9-11, "said phases of said clock signal, circuitry for receiving serial data, and circuitry" should be "said phases of said clock signal and said serial data, said circuitry". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Tash et al.

Tash et al. (US Patent No. 5,127,023) discloses a retimer 58 in a receiver circuit is shown in Figure 4.

Referring to Figure 4, the retimer 58 comprises at least a clock generating circuit 56; a clock generation and control circuit 78 for generating a multi-phase clock A2 and a complement of the multi-phase clock A2 from a clock generated by the clock generating circuit 56; a pair of end of frame detection shift registers 74 and 75 serially shift the DATA and the complement of the DATA generated by a data reshaping and sync transition detection circuit 72 and the clock A2 and the complement of the clock A2 to detect a sampling clock edge in Manchester data cell in order to avoid the transition that always occurs at the midpoint (col. 7, lines 4-28); an end of frame detection circuit 76 to detect active RESET signals (col. 7, lines 50-63); and a NAND gate 82 to output retimed data (col. 7, line 68 to col. 8, line 4).

Figure 5 shows the detailed embodiments of the data reshaping and sync transition detection circuit 72 and the clock generation and control circuit 78 of Figure 4.

Figure 6 shows the detailed embodiments of the pair of end of frame detection shift registers 74 and 75 of Figure 4.

With respect to claim 1 and claim 7, the phases of the clocks A2 are generated by the clock generation and control circuit 78; and the circuits (74-76 and 82) of the retimer 58 for receiving the DATA, the complement of the DATA, the clock A2 and the complement of the clock A2 to reduce timing uncertainties in the serial data by outputting a value of the serial data sampled at a particular phase of the clock which is the nature of the goal for generating a retimed data in a retiming circuit. In claim 7,

Tash teaches that the DATA and the complement of the DATA are derived from a transceiver 52, but does not explicitly show or suggest the transmitter of the transceiver 52 converts a parallel data into the serial data. As mentioned in the background information on pages 1 and 2 of the instant application, it is well known to a person skill in the art that the serial data of a receiver is derived from a transmitter for converting parallel data into serial data before transmitting the serial data to the receiver through a transmission medium.

With respect to claims 2-3 and 8-9, in Figure 6, each of the end of frame detection shift registers 74 and 75 corresponds to the second unit having D flip-flops for sampling the DATA by the clock A2 and the complement of the clock A2.

With respect to claims 4-6 and 10-12, in Figure 6, the NAND gate 110 and the AND gate 113 together operate as one of the second units, and the NAND gate 111 and the AND gate 113 together operate as another one of the second units associated with the pair of end of frame detection shift registers 74 and 75. The NAND gates 110 and 111 are combined with the outputs of the D flip-flops and output logic states to the AND gate using the phases of the clock A2 and the complement of the clock A2.

6. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Jung et al..

Jung et al. (US Patent No. 5,887,040) discloses a high speed digital data retiming apparatus in a receiver circuit is shown in Figure 2.

Referring to Figure 2, the retiming apparatus comprises a clock generating circuit 201 for generating a multi-phase clock from an external clock; a clock selection circuit

202 for selecting clock signals of serial data; a retiming synchronization circuit 203 for selecting a synchronized clock pulse; a data retiming circuit 204 for generating retimed data of the serial data based on the synchronized clock pulse; and a an elastic buffer 205 for generating retimed serial data of the retimed data based on the external clock. See col. 3, line 42 to col. 4, line 6.

Figure 3 shows the detailed embodiment of the clock generating circuit 201 of Figure 2.

Figures 5-7 show the detailed embodiment of the clock selection circuit 202 of Figure 2 to generate normal phase clock select signals and inverse phase clock select signals which is the complement of the normal phase clock select signals. See col. 6, lines 24-51.

Figure 10 shows the detailed embodiment of the retiming synchronization circuit 203 of Figure 2.

With respect to claim 1 and claim 7, the serial data is provided to an input of the clock selection circuit 202 and the data retiming circuit 204; the phases of the external clock are generated by the clock generating circuit 201; the retiming synchronization circuit 203 and the data retiming circuit 204 of the retiming apparatus for reducing timing uncertainties in the serial data by outputting a value of the serial data sampled at a particular phase of the clock which is the nature of the goal for generating a retimed data in a retiming apparatus. In claim 7, although Jung does not explicitly show or suggest where is the serial data derived from. As mentioned in the background information on pages 1 and 2 of the instant application, it is well known to a person skill

in the art that the serial data of a receiver is derived from a transmitter for converting parallel data into serial data before transmitting the serial data to the receiver through a transmission medium.

With respect to claims 2-3 and 8-9, in Figure 10, the retiming synchronization circuit 203 comprises a plurality of logic gates corresponding to the first units for sampling the serial data using clock signals and the complement of the clock signals generated by the clock selecting generator 202 (also see Figures 3 and 5-7).

With respect to claims 4-6 and 10-12, in Figures 6 and 7, all the block elements are operated in logic circuits and corresponded to the second units to generate a combinational logic using the phases of the clock signals and the complement of the clock signals.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

References Buckner et al., Chen, and Dalmia are related to retiming or recovery data circuits in a receiver circuit for generating a retimed or recovered data and clock based on a selected phase of a plurality phases of a clock.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Young Tse** whose telephone number is **(703) 305-4736**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Jay Patel**, can be reached at **(703) 308-7728**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Young T. Tse
Primary Examiner
8/8/04